

J&W Electronics Co.,LTD

Board name: Mother Board Schematic
Project name: C116
Version: VerA
initial Date: 2011-03-13
New update:

1. System Block Diagram & Schematic page description;
2. Power Block Diagram & Discription;
3. Annotations & information;
4. Schematic modify Item and history;
5. Power on & off Sequence;
6. ACPI Mode Switch Timings;
7. Power On Sequence Map;
8. CLOCK Distribution;
9. Power Distribution;

J&W Confidential

Hardware drawing by:

Hardware check by:

EMI Check by:

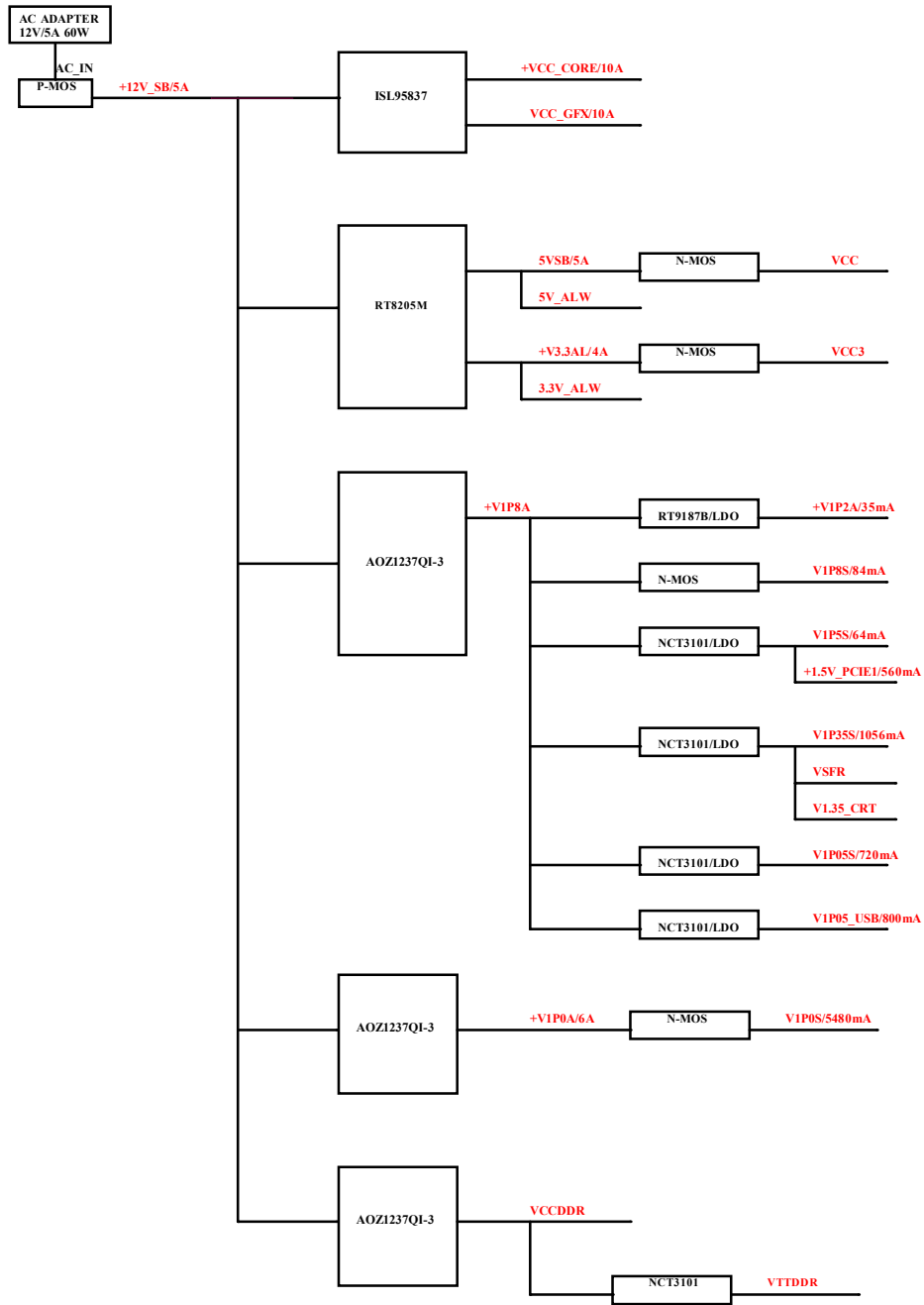
Power drawing by:

Power check by:

Manager Sign by:

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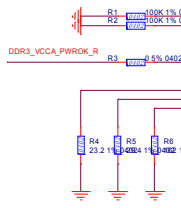
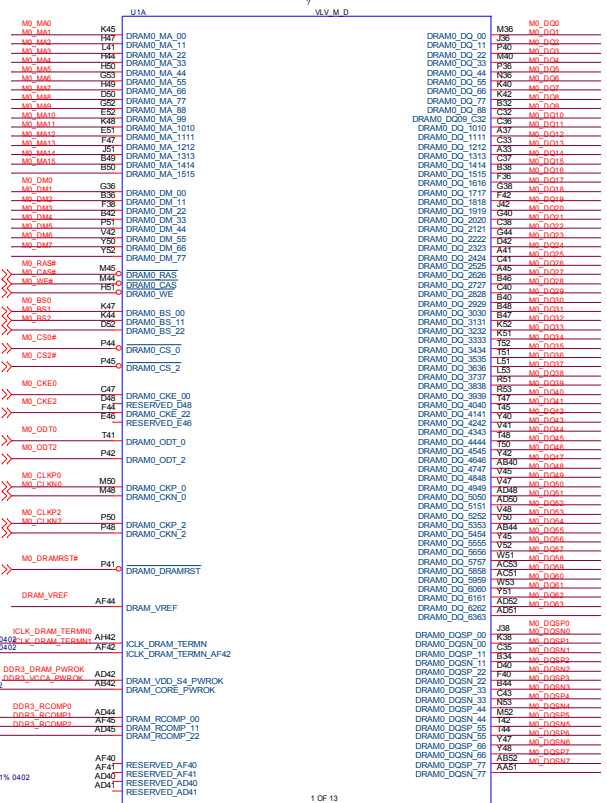
POWER SEQUENCE



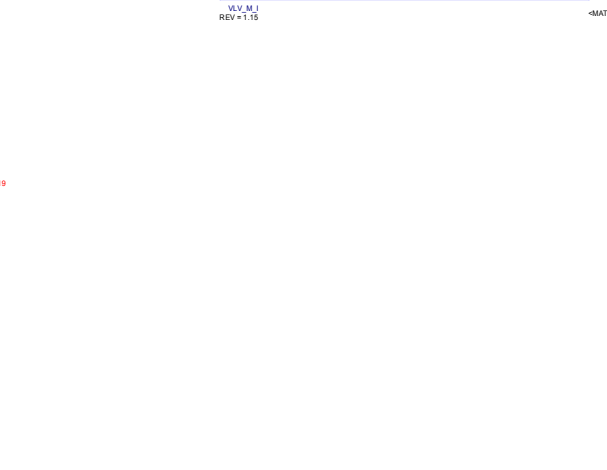
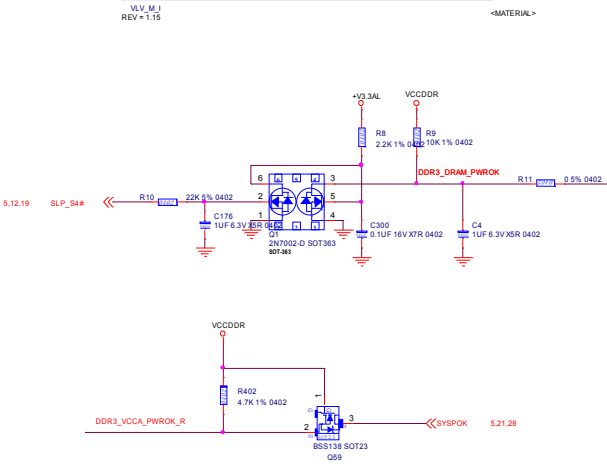
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>>>M0_DQSP[7:0] 8
 >>>M0_DQSN[7:0] 8
 >>>M0_DQ[63:0] 8
 >>>M0_MA[15:0] 8
 >>>M0_DM[7:0] 8

>>>M1_DQSP[7:0] 8
 >>>M1_DQSN[7:0] 8
 >>>M1_DQ[63:0] 8
 >>>M1_MA[15:0] 8
 >>>M1_DM[7:0] 8



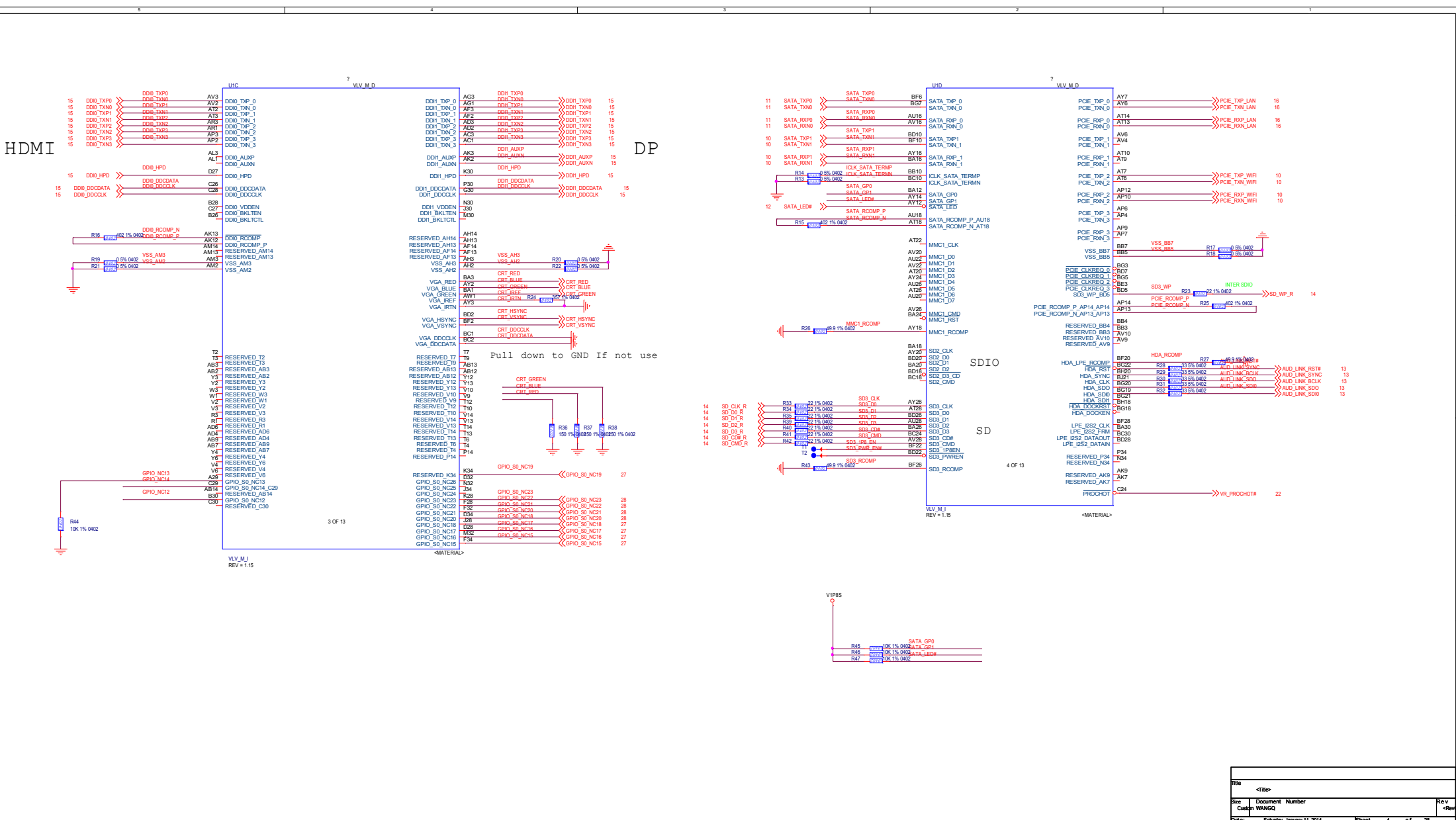
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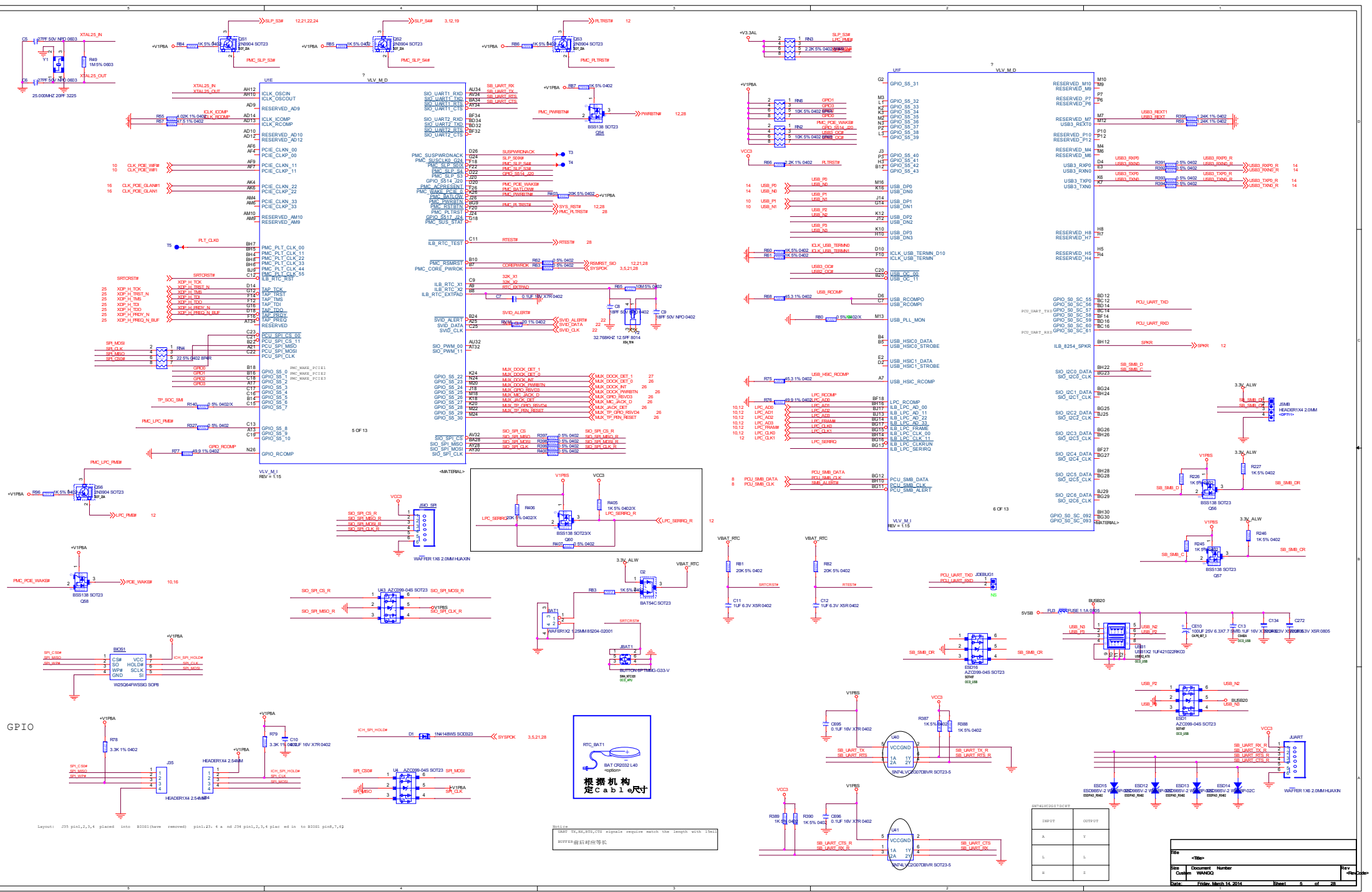
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HDMI

DP



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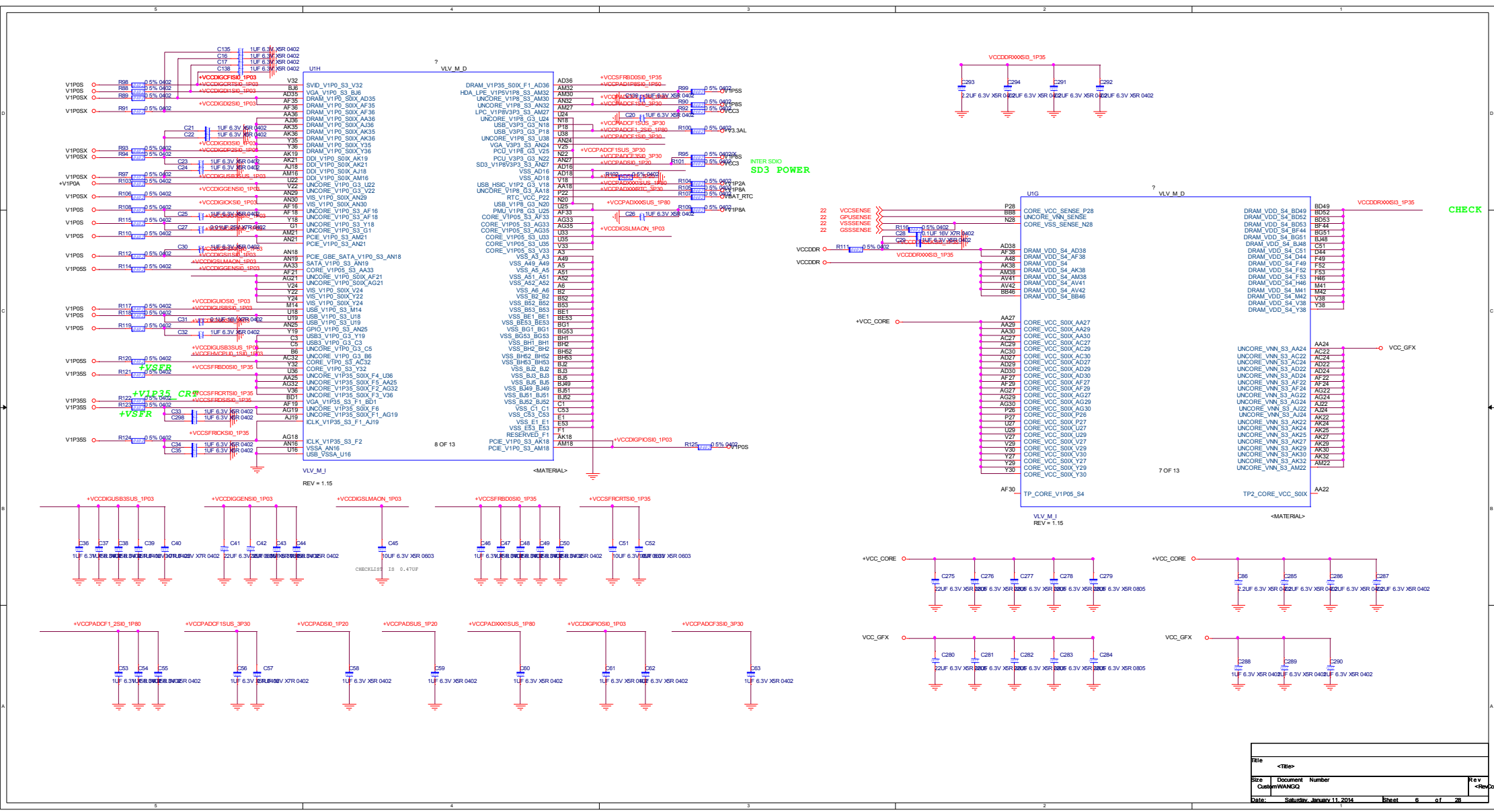


Layout: 238 pin1,2,3,4 placed into B001(these removed) pin1,2, 4 + net 234 pin1,2,3,4 placed in to B001 pin1,7,2

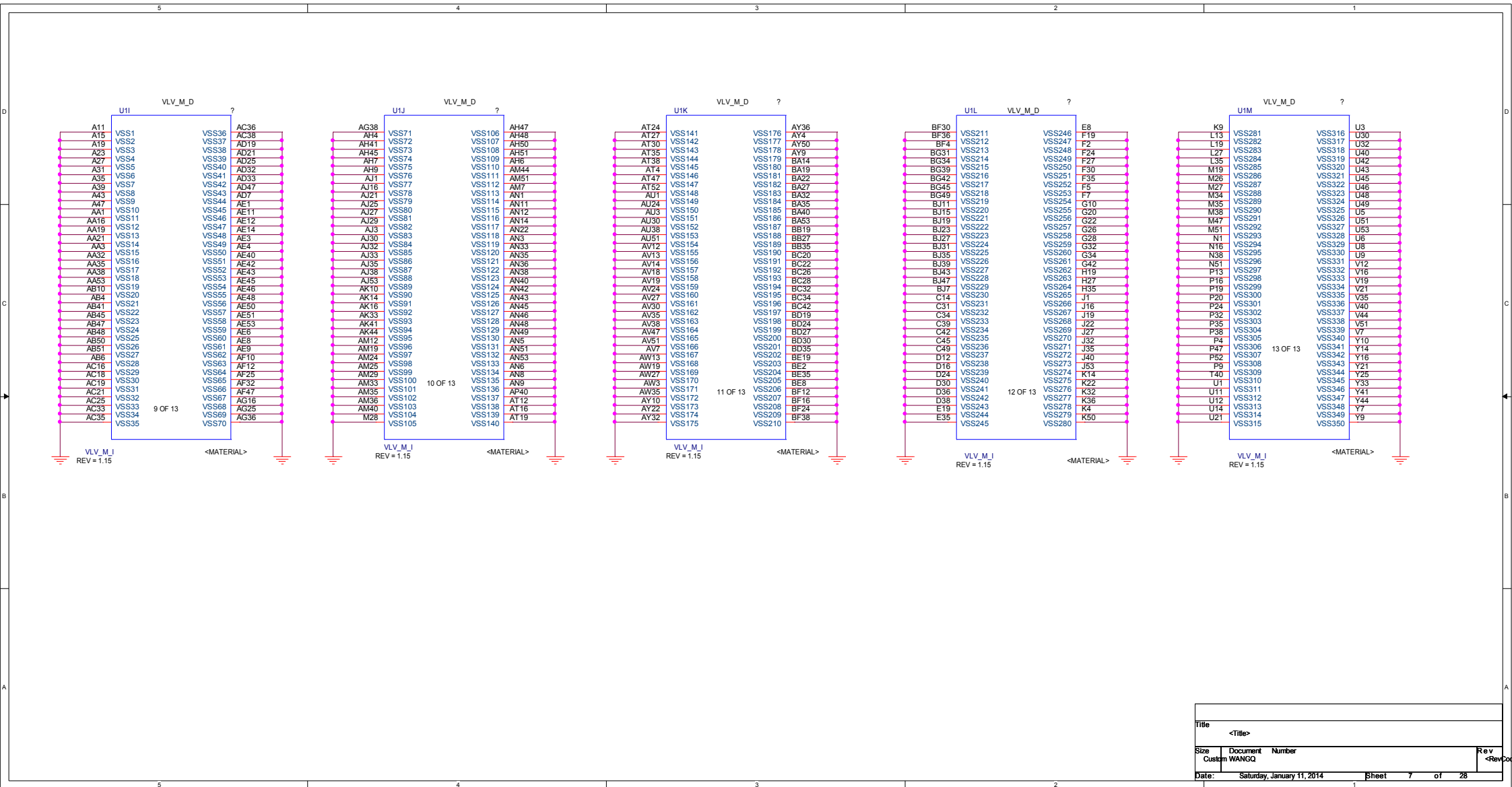
根据机构定c a b l e尺寸

011110 12,16,20,24,28 signals require match the length with 15ohm
SMT07 前后对称等长

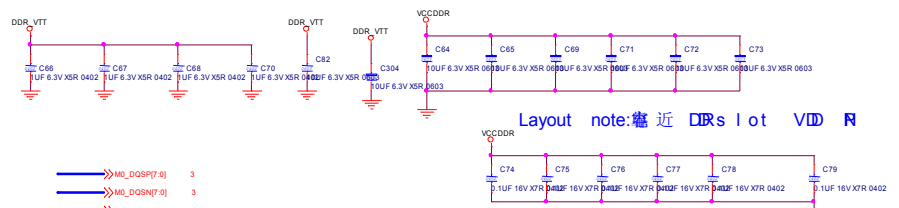
INPUT	OUTPUT
A	Y
L	L
S	S



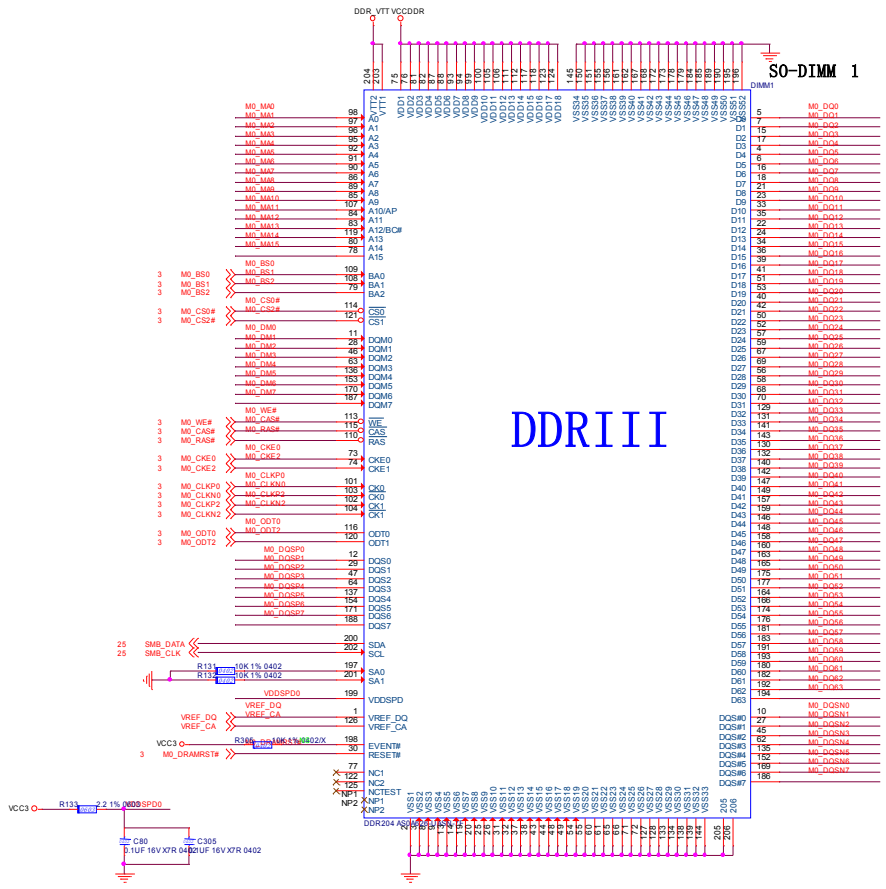
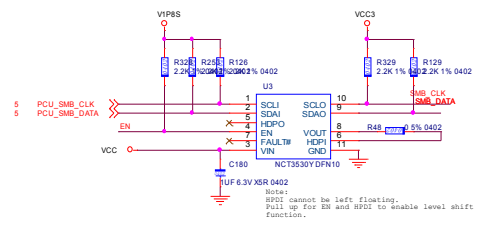
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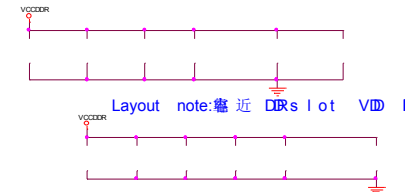
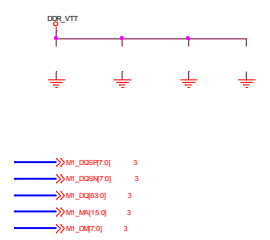


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- >>M0_DQSP1[7:0] 3
- >>M0_DQSN1[7:0] 3
- >>M0_DQ[8:3:0] 3
- >>M0_MA[15:0] 3
- >>M0_DM[7:0] 3



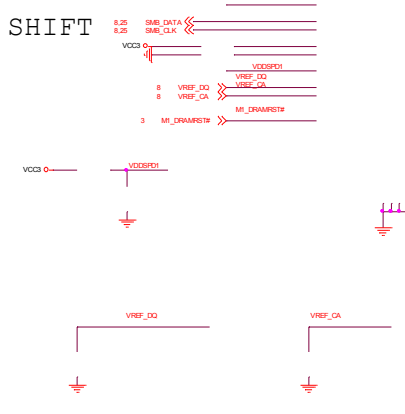


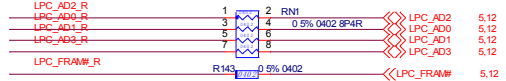
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- MI_DQSF1[1] 3
- MI_DQSF1[2] 3
- MI_DM15[0] 3
- MI_DM15[1] 3

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		MI_M02		MI_D02
		MI_M03		MI_D03
		MI_M04		MI_D04
		MI_M05		MI_D05
		MI_M06		MI_D06
		MI_M07		MI_D07
		MI_M08		MI_D08
		MI_M09		MI_D09
		MI_M10		MI_D10
		MI_M11		MI_D11
		MI_M12		MI_D12
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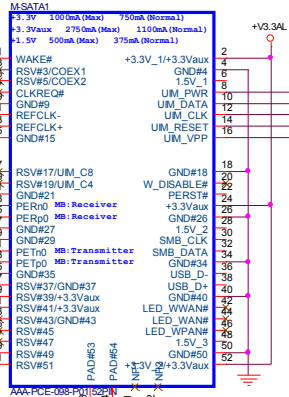
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LEVEL SHIFT

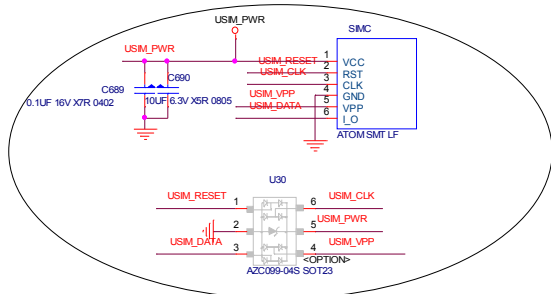
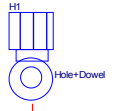
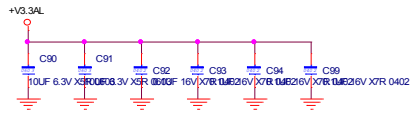
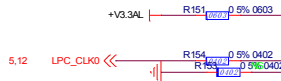
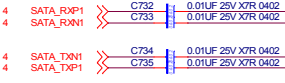




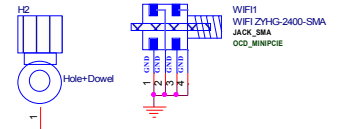
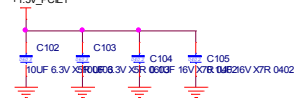
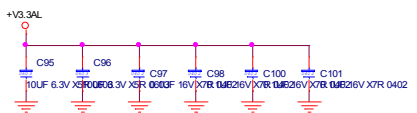
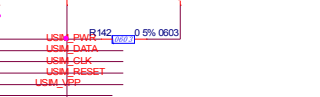
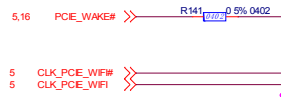
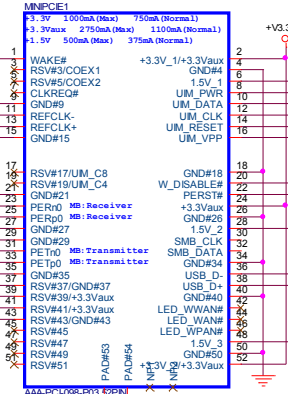
MINI-PCIE V1.2 SPEC;



P N CHANGE FOR MSATA

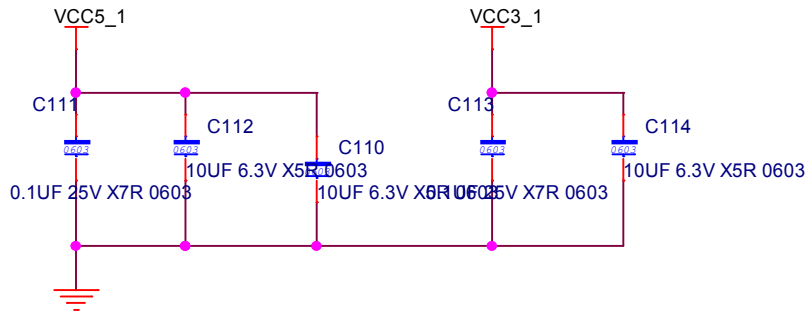
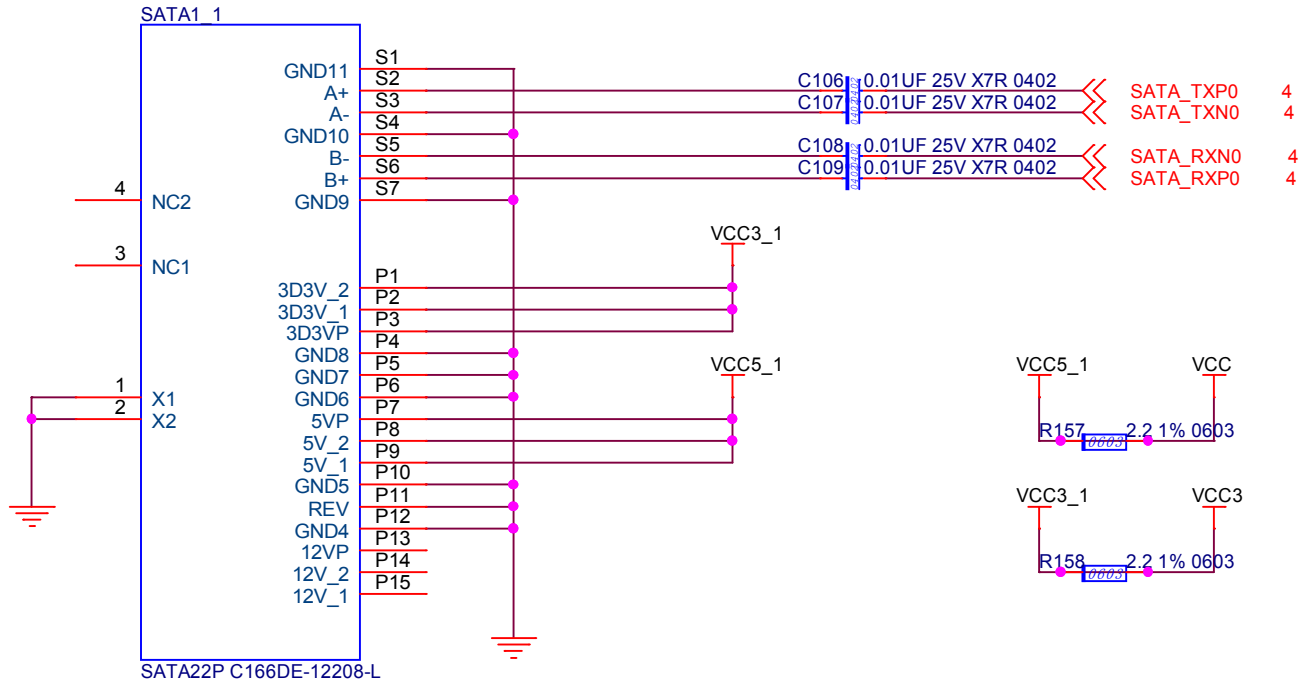


MINI-PCIE V1.2 SPEC;

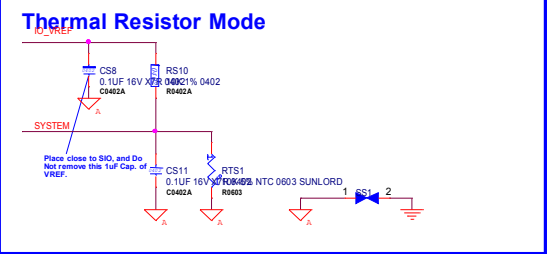
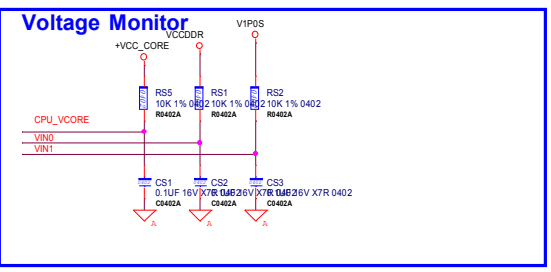
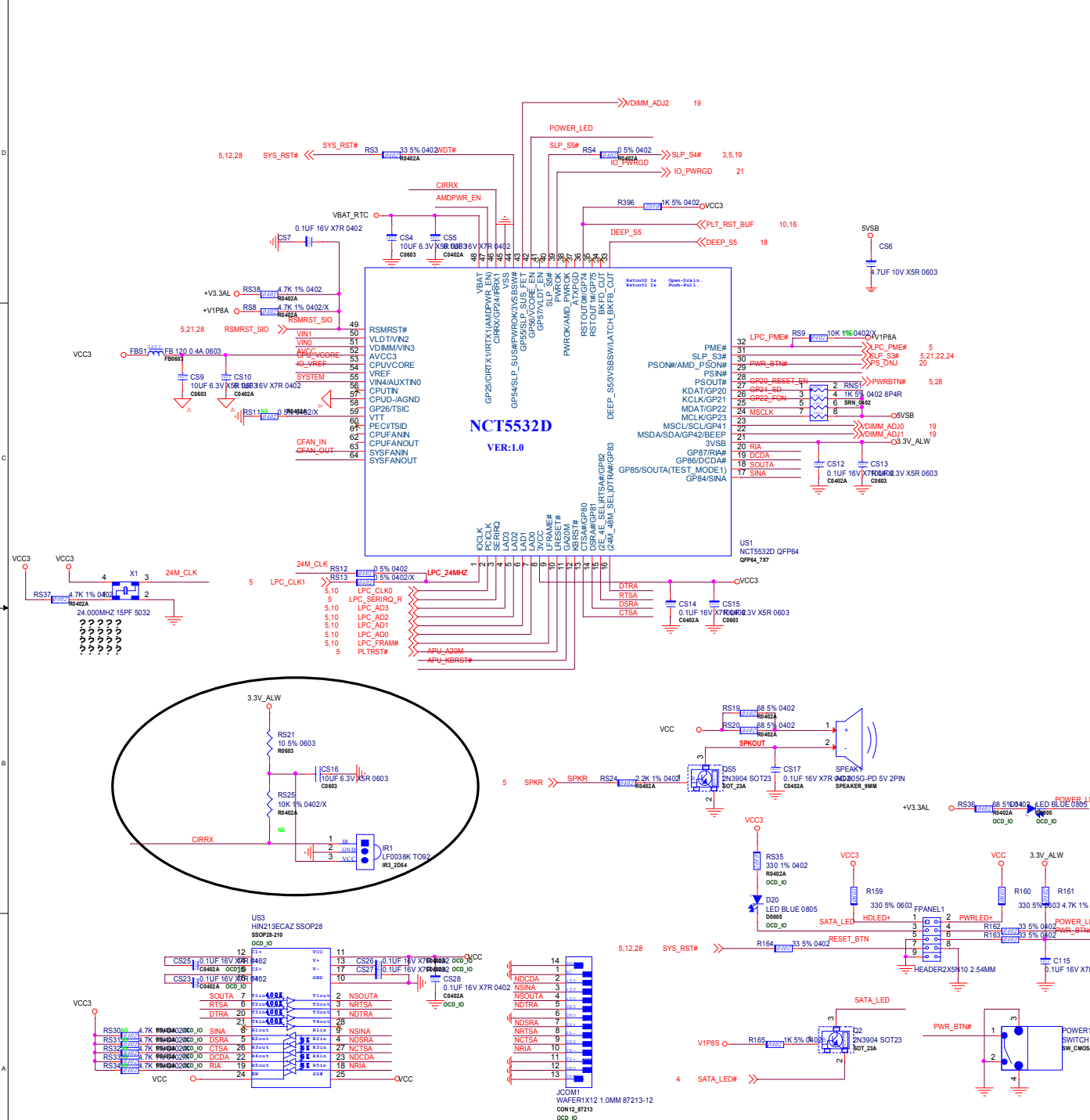


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SATA CONNECTOR

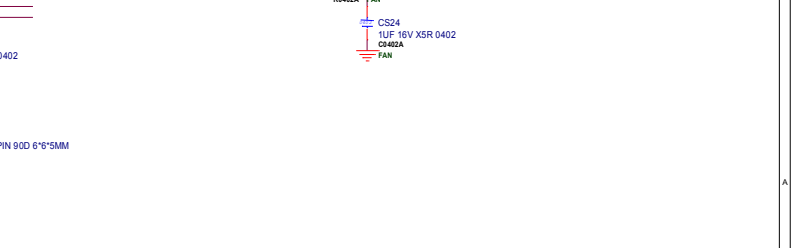
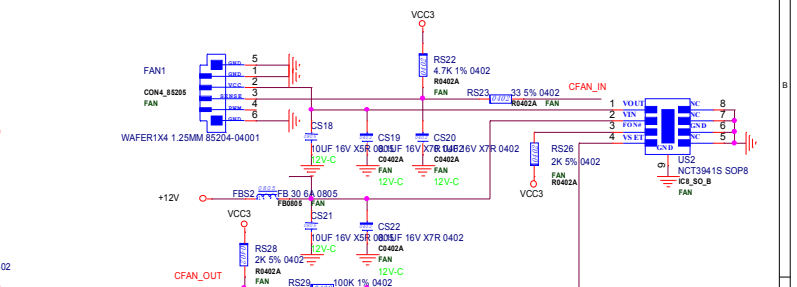
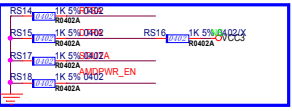


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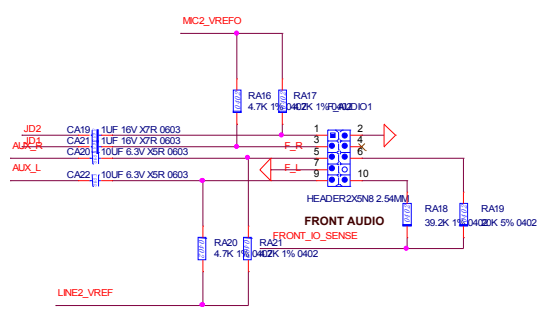
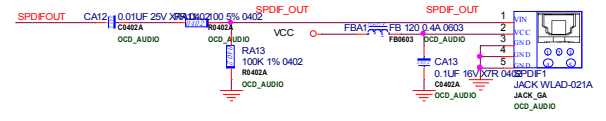
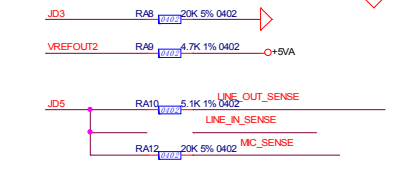
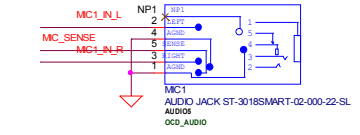
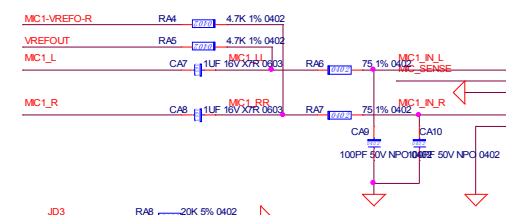
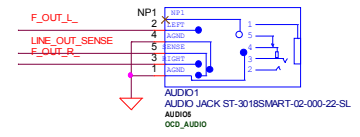
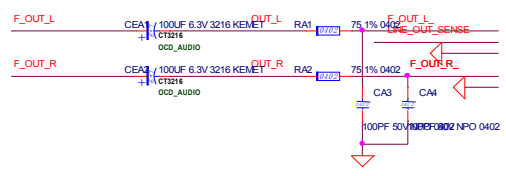
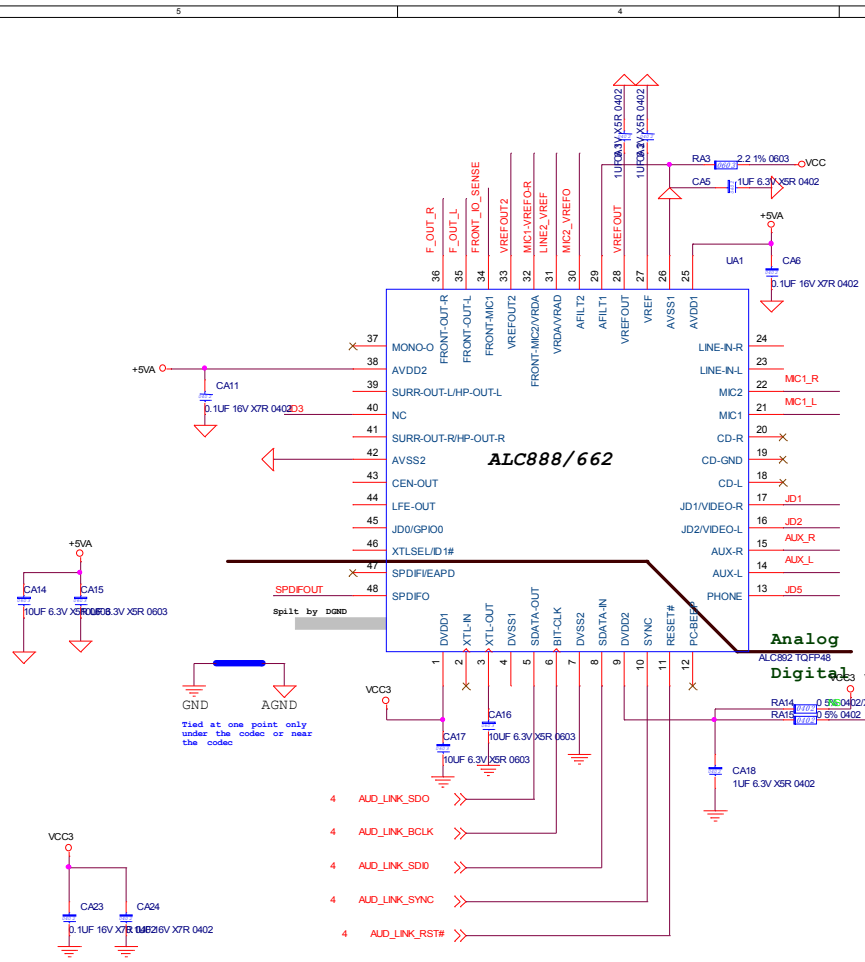


Power On Strapping

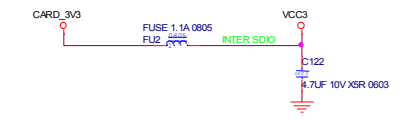
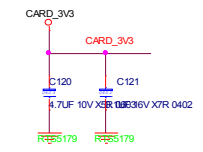
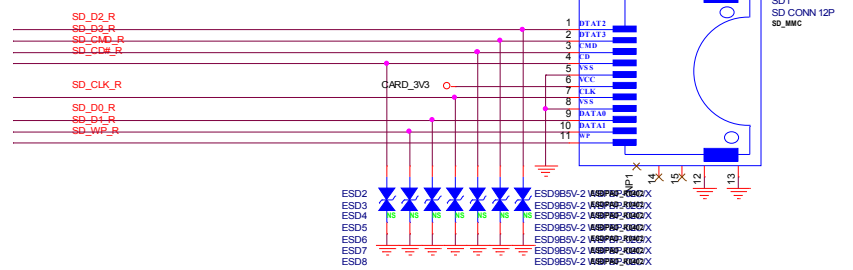
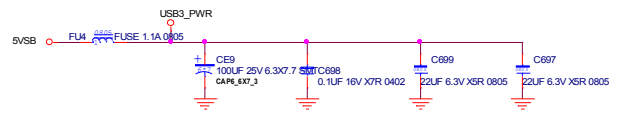
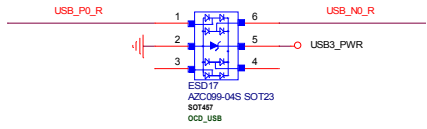
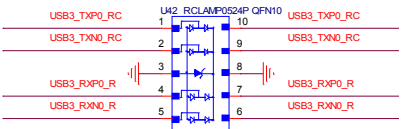
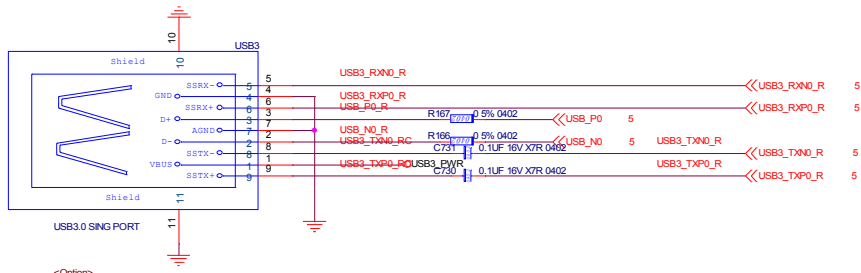
PIN15/RTSA	2E_4E_SEL	Strapped by LRESET#	1 4Eh/4Fh 0 2Eh/2Fh
PIN16/DTRA	24M_48M_SEL	Strapped by VCC	1 48MHz 0 24MHz
PIN18/SOUTA	TEST_MODE1	Strapped by VCC	strapped to low
PIN47	AMDPWR_EN	Strapped by VSB	1 Enable 0 Disable



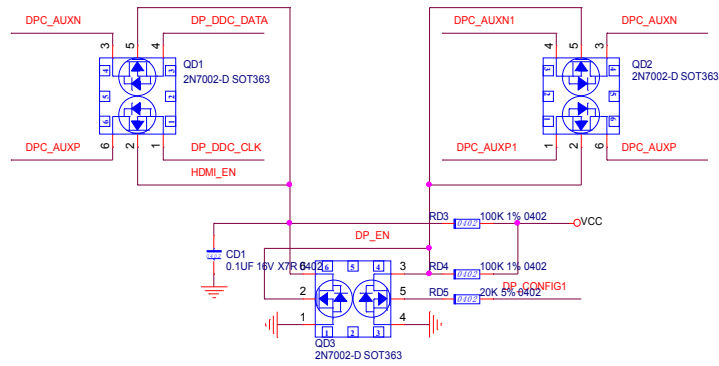
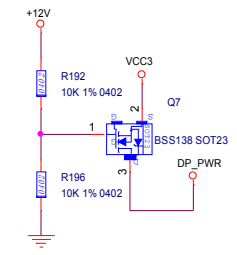
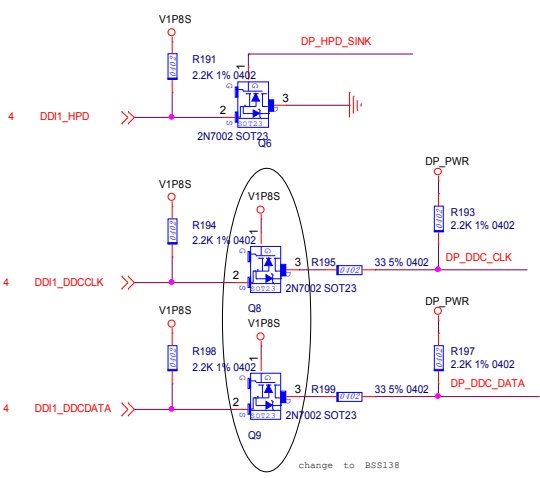
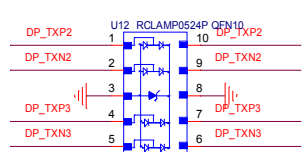
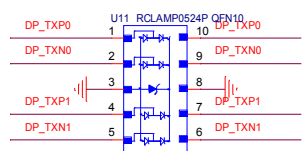
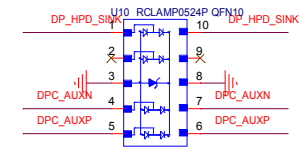
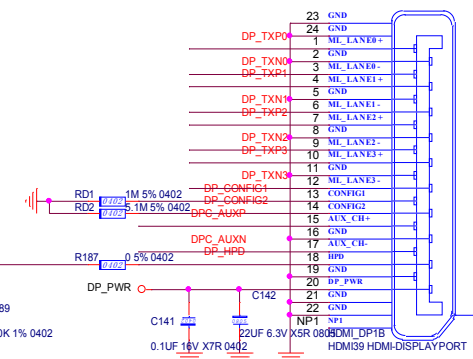
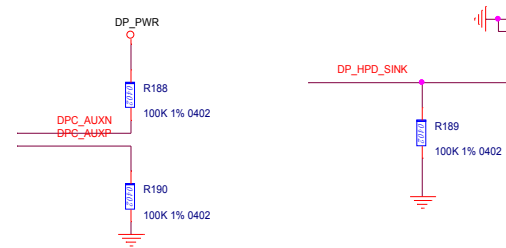
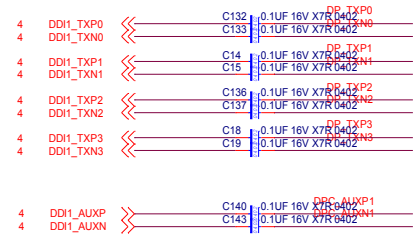
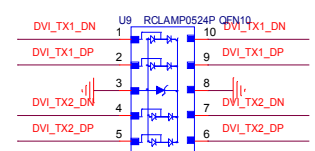
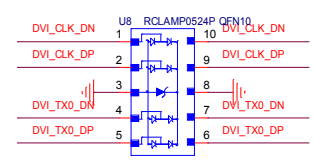
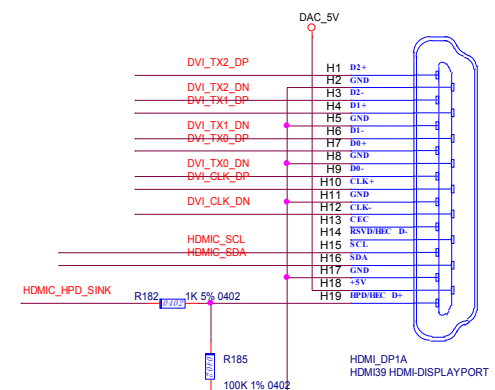
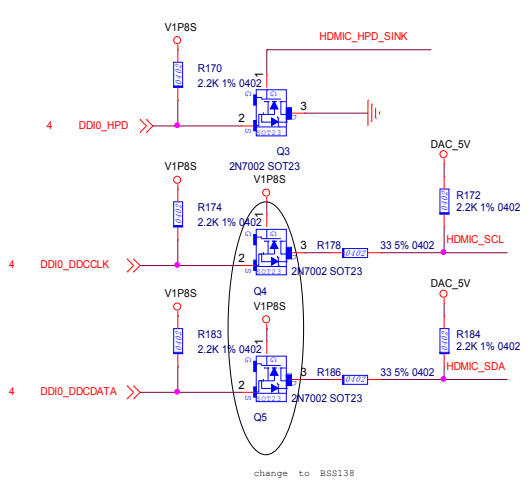
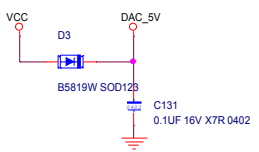
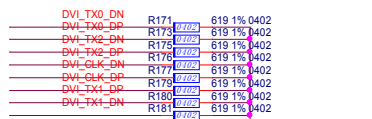
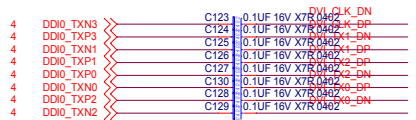
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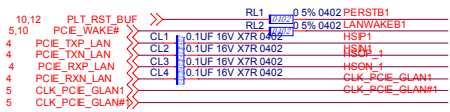
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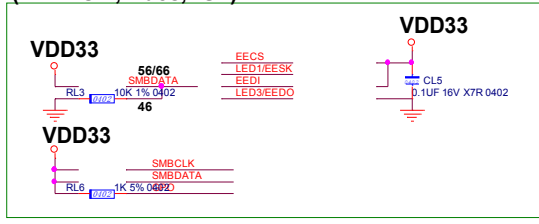
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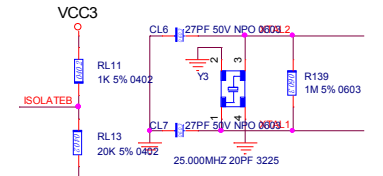
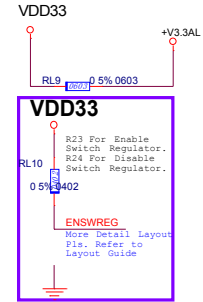
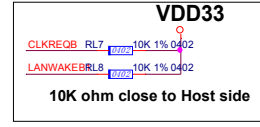
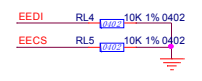
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Function (EEPROM, Efuses, ASF)



Pin44-XTAL2 is External Clock Input Pin. R38 is needed when using external clock source.



For RTL8111B-VB
* C12 to C17 are for VDD33 pins-- 12, 27, 39, 42, 47, 48.

For RTL8105E-VB
* C12 to C16 are for VDD33 pins-- 27, 39, 42, 47, 48.

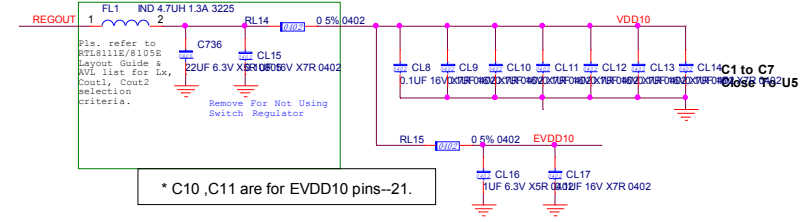
For RTL8105E-VC
* C12 to C15 are for VDD33 pins-- 27, 39, 47, 48.

For RTL8111B-VB
* C1 to C7 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

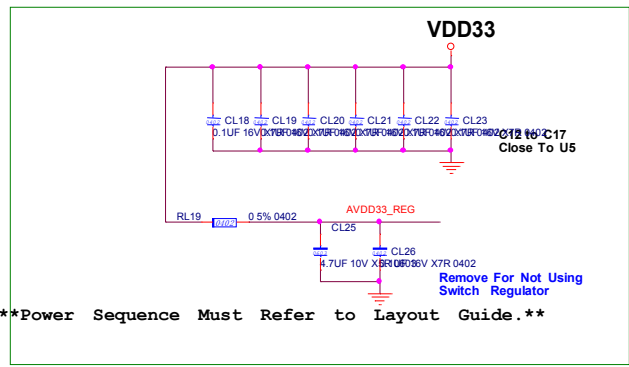
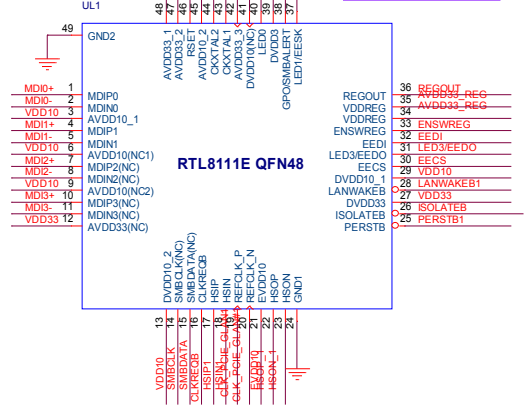
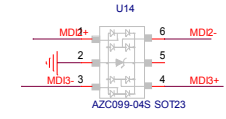
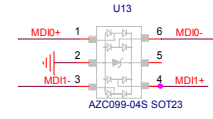
For RTL8105E-VB
* C1 to C4 are for VDD10 pins-- 3, 13, 29, 45.

For RTL8105E-VC
* C1 to C3 are for VDD10 pins-- 13, 29, 45.

External 1.05V Supply When Not Using Switch Regulator. If Using External 1.2V Supply Pls. Contact With P&E.

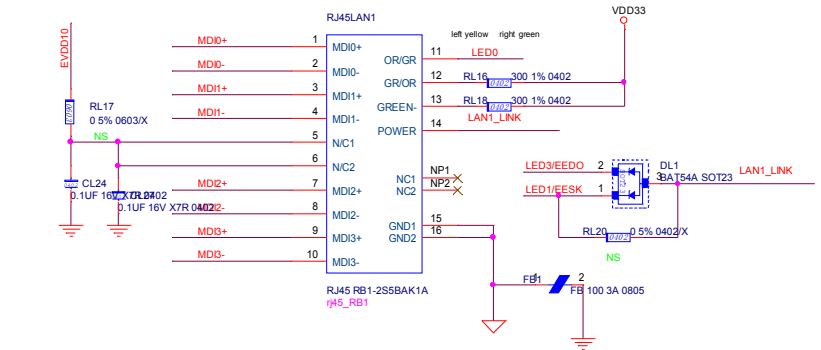


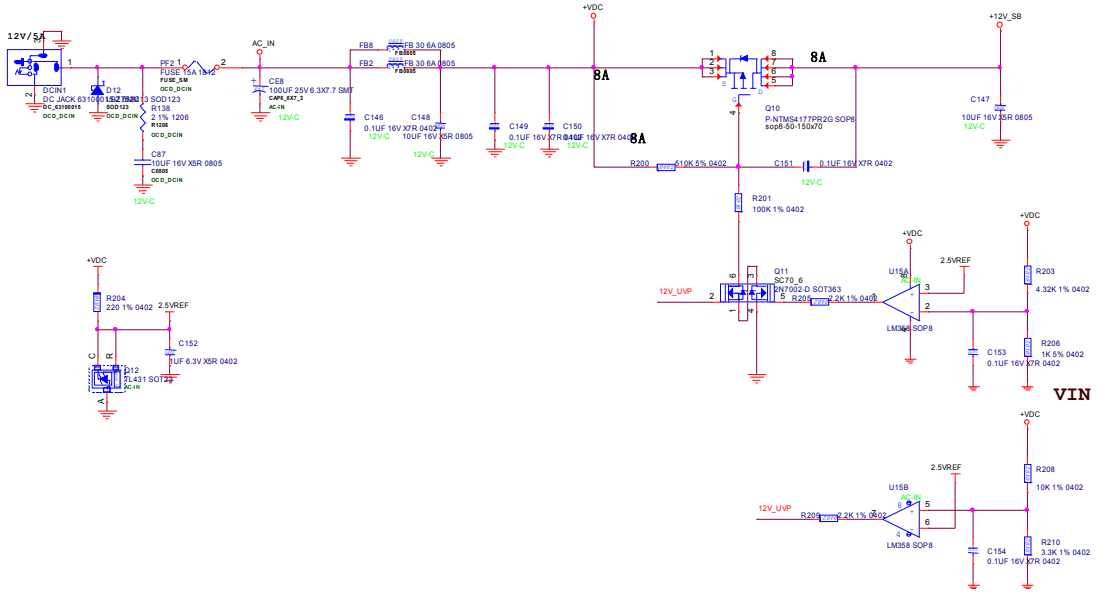
* C10, C11 are for EVDD10 pins--21.



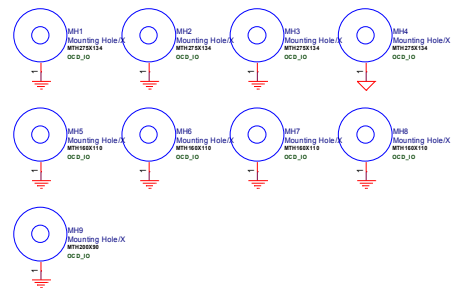
Power Sequence Must Refer to Layout Guide.

C10, C11 Close To U5 Pin 21.	mode	Lx	Cout1,2	R1	Cin1,2	R3	R23	R24
8111E-VB/8105E-VB/8105E-VC	SWR	O	O	O	O	O	O	X
8105E-VC	LDO	X	X	X	X	X	X	O
8111E-VB/8105E-VB	External	X	X	X	X	X	X	O
8105E-VC	External	X	X	X	X	X	O	X

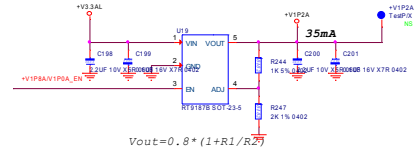
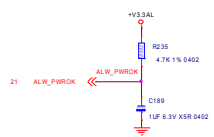
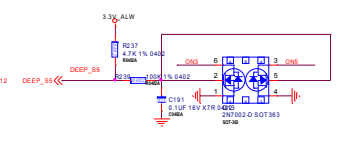
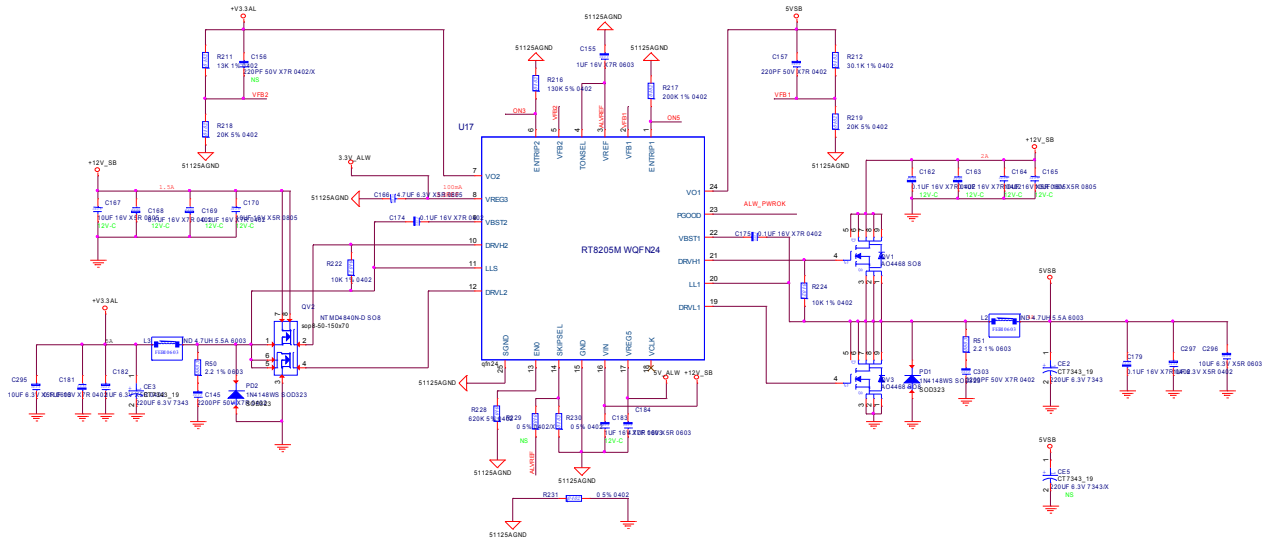




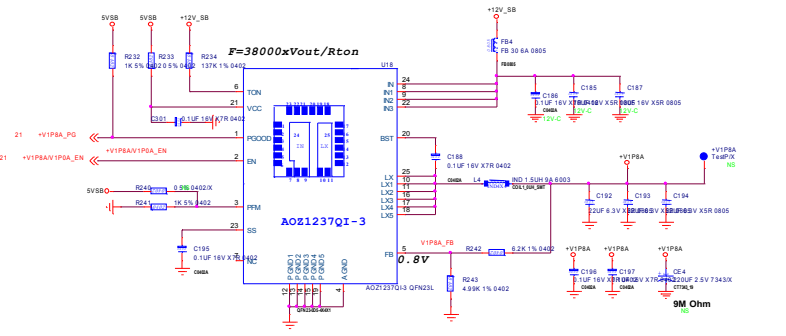
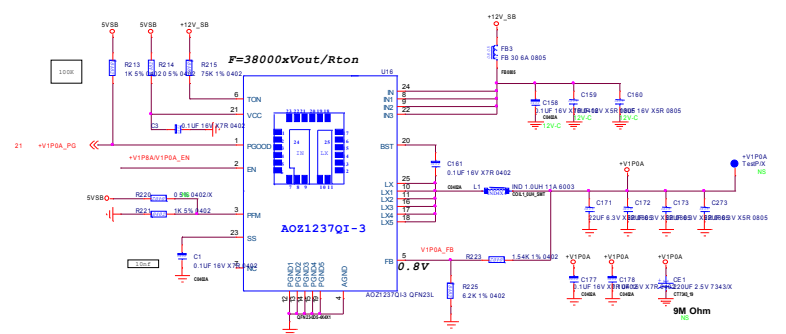
VIN MAX 13.2V
 MIN 10.2V



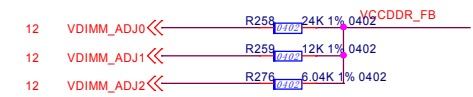
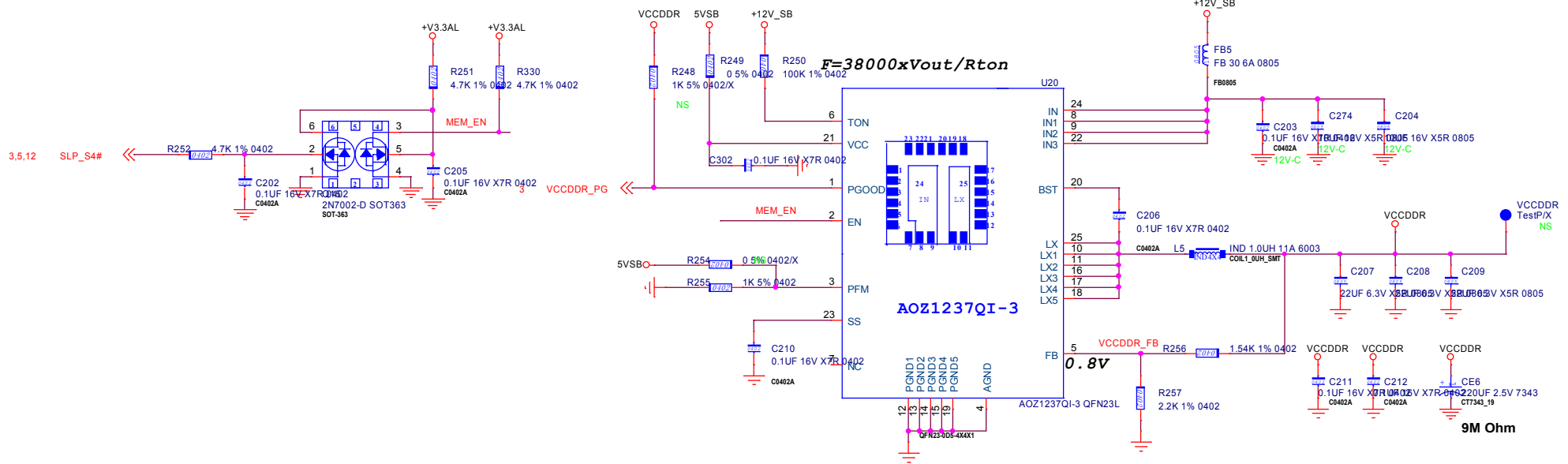
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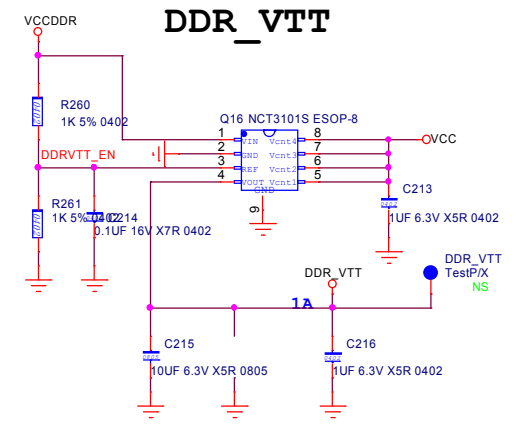
$$V_{out} = 0.8 * (1 + R1/R2)$$



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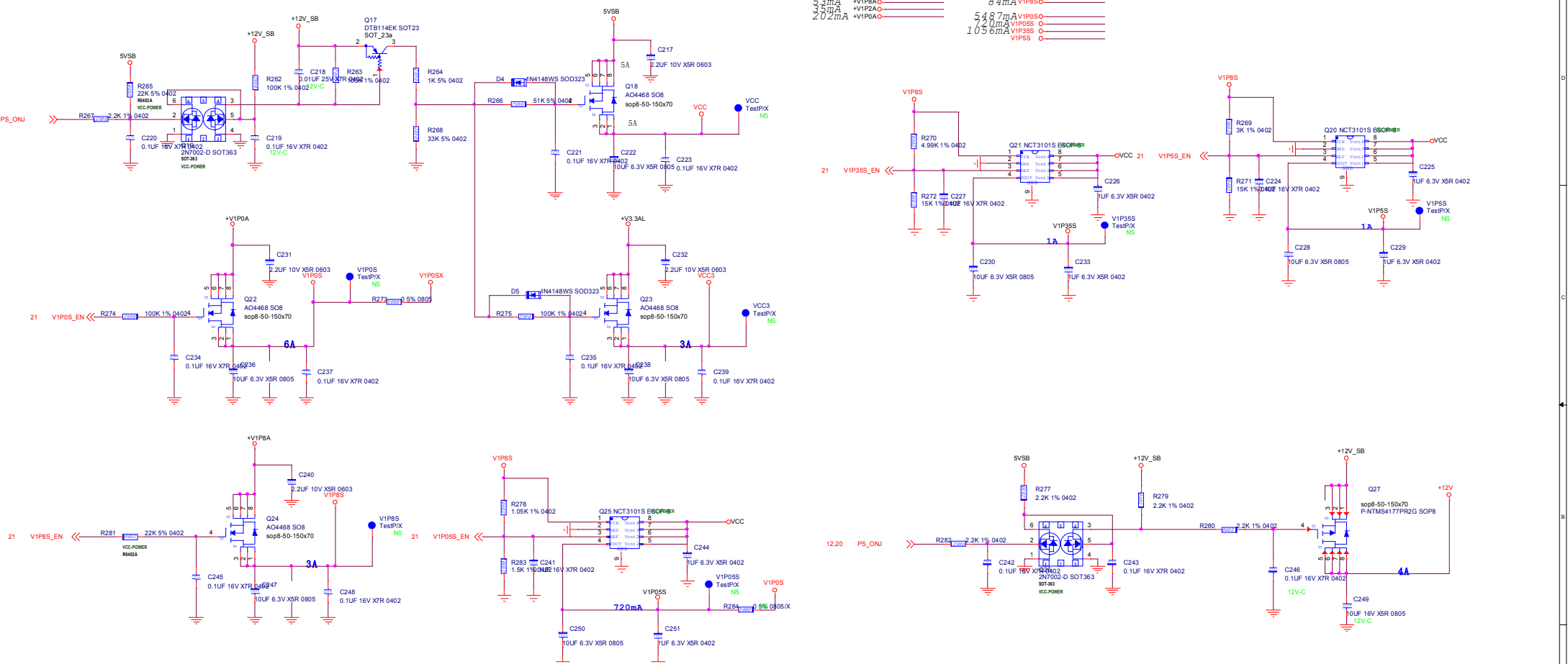


1.36---1.71v

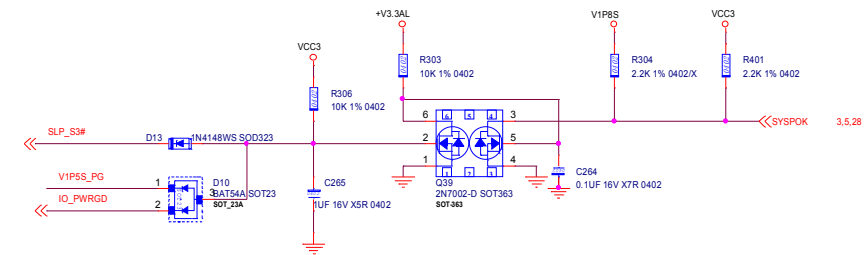
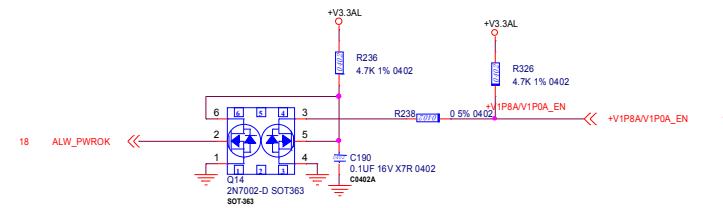
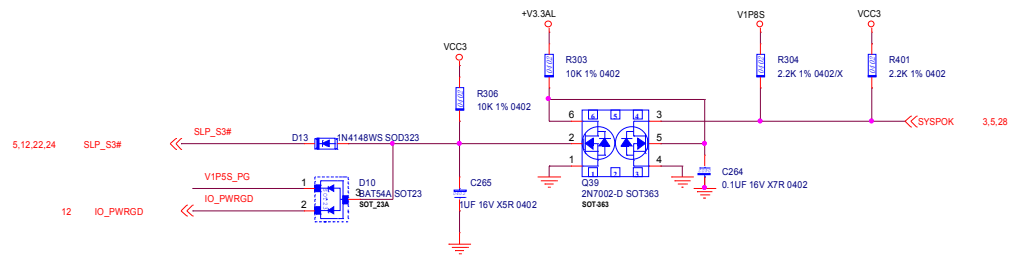
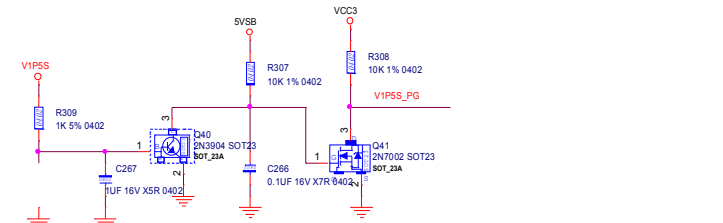
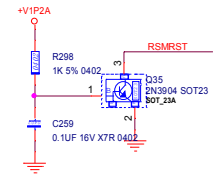
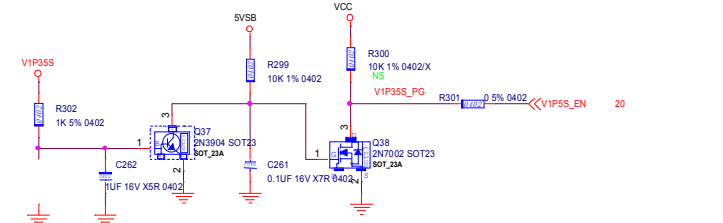
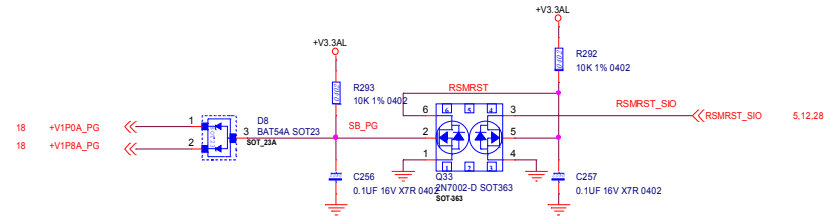
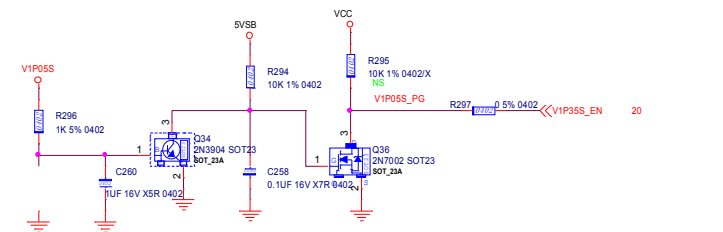
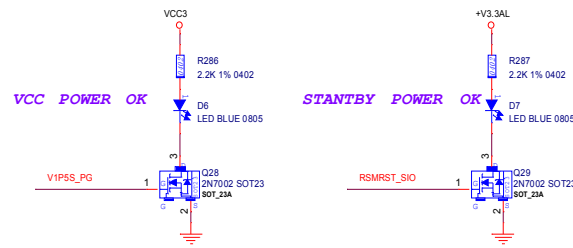
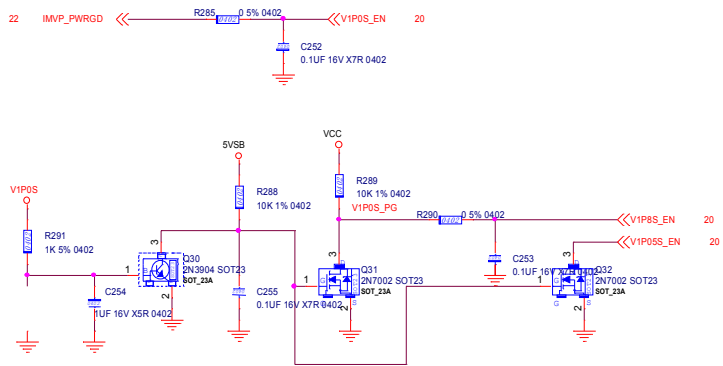


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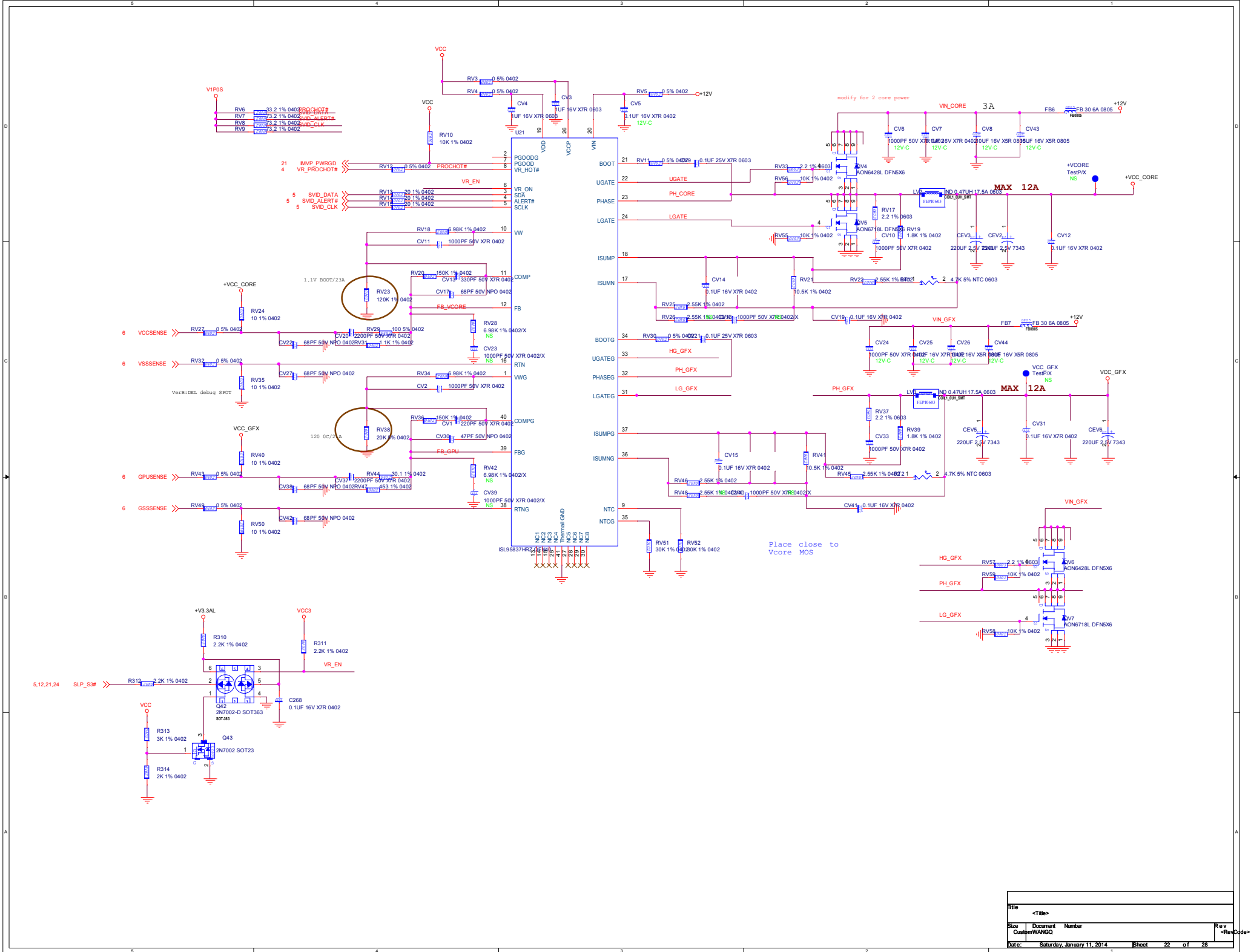
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 +V3.3AL 0 mA
 +V1P8A 0 mA
 +V1P2A 0 mA
 +V1P0A 0 mA
 8 mA V1P8S
 54.87 mA V1P8S
 7.20 mA V1P3SS
 105.6 mA V1P3SS
 V1P8S
 V1P3SS



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D

D

C

C

B

B

A

A

5

4

3

2

1

5

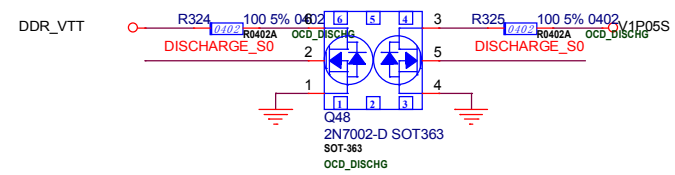
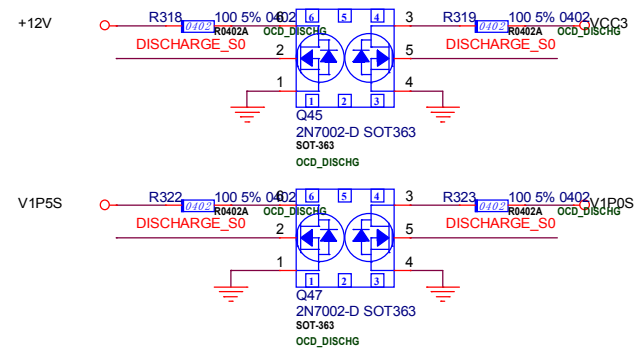
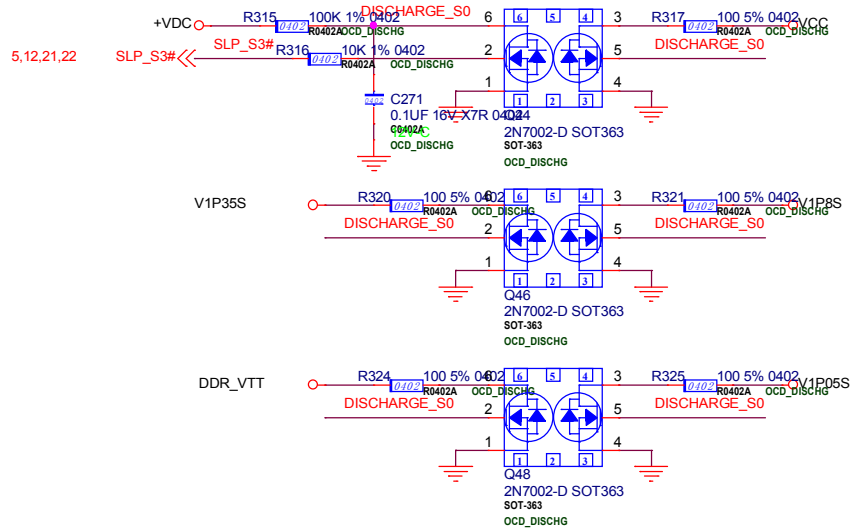
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3

2

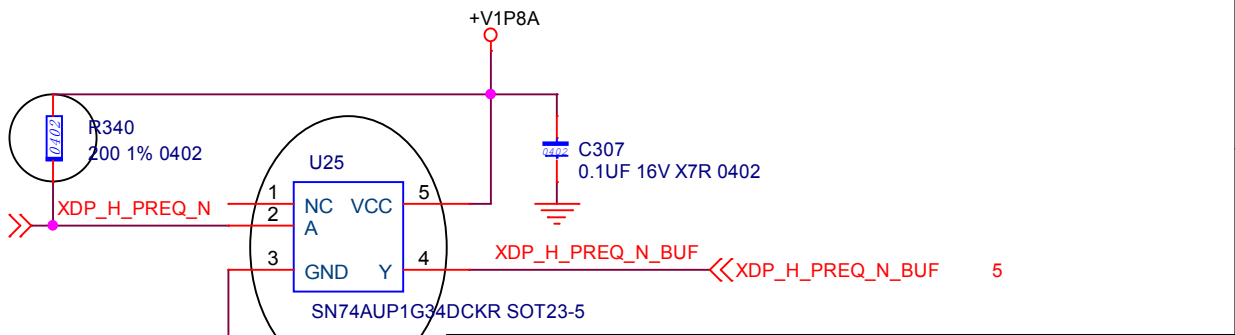
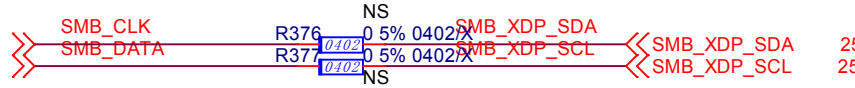
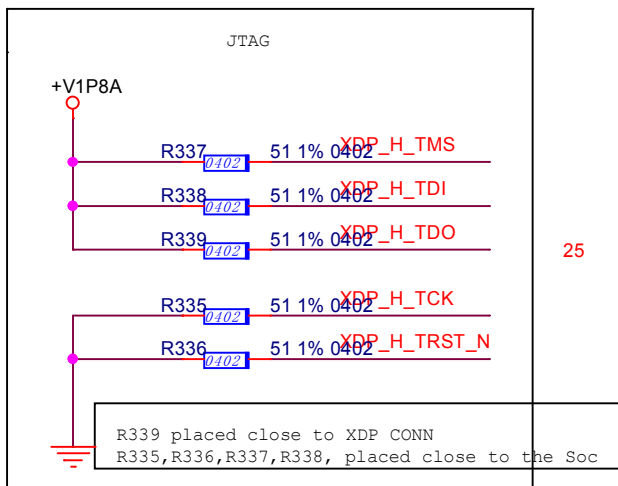
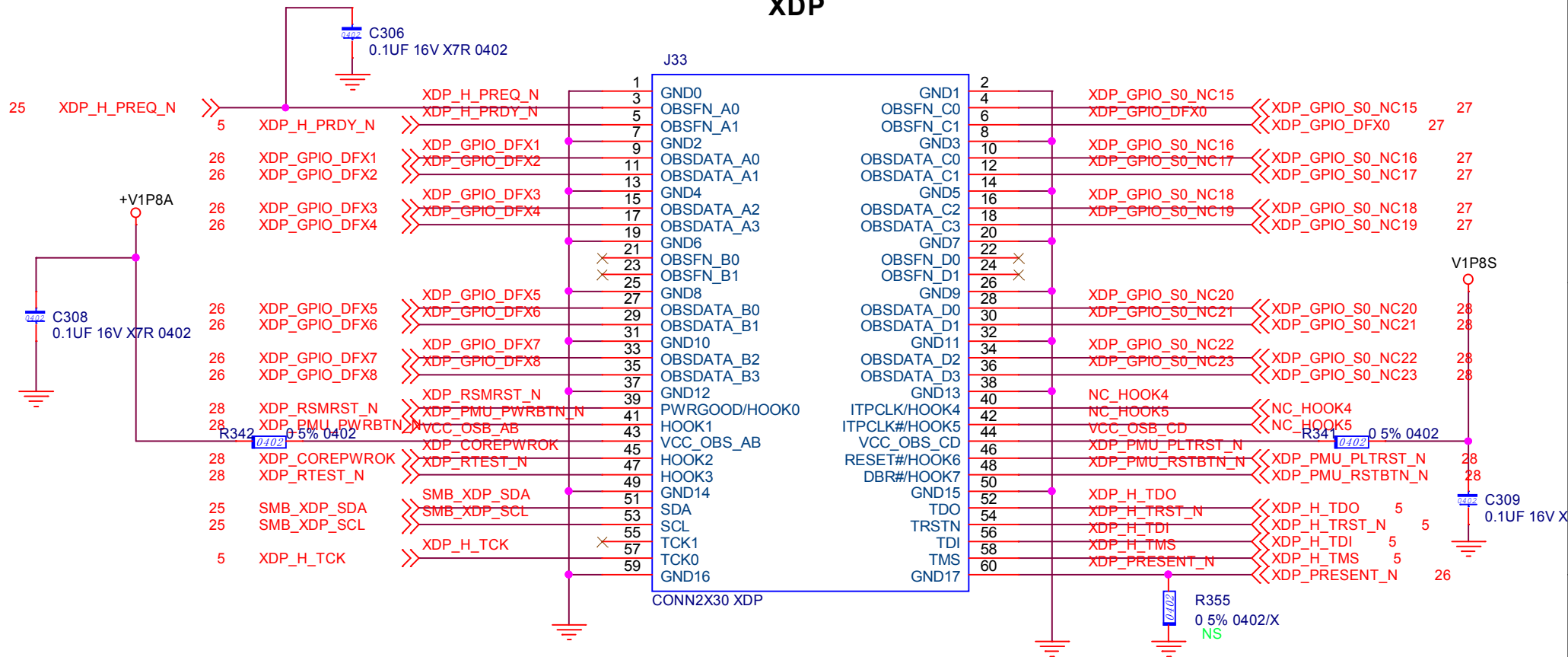
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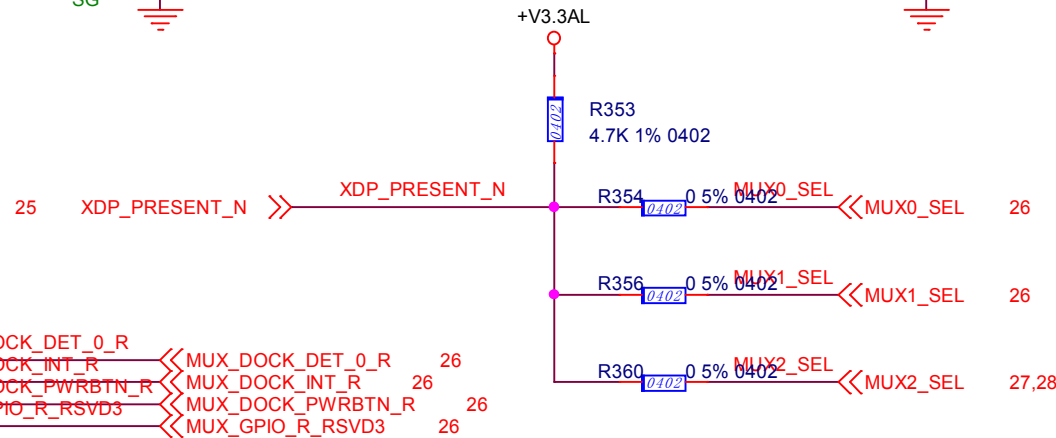
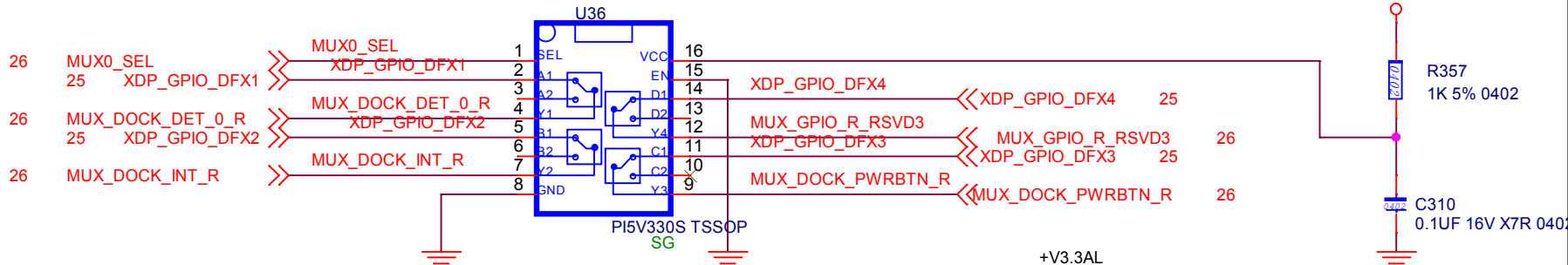
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XDP

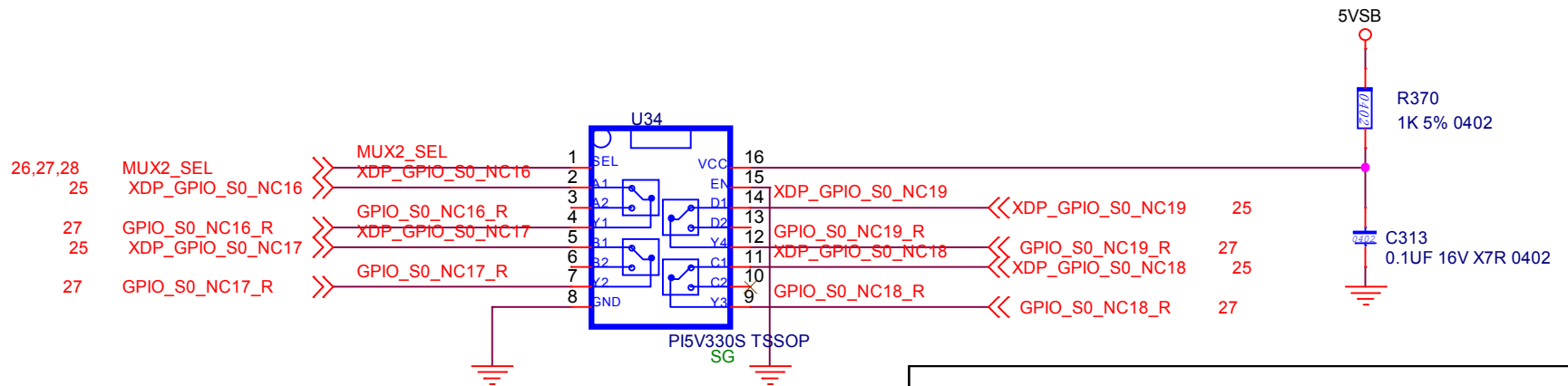
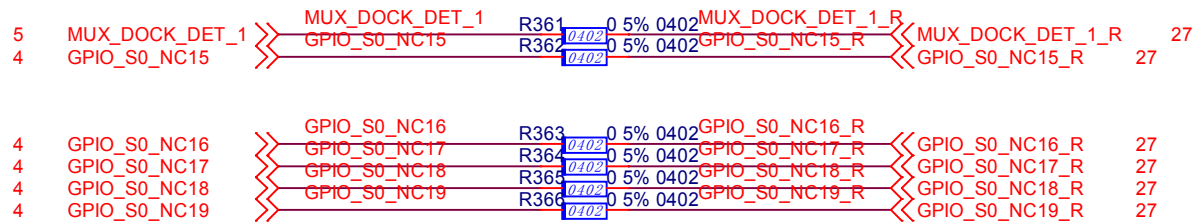
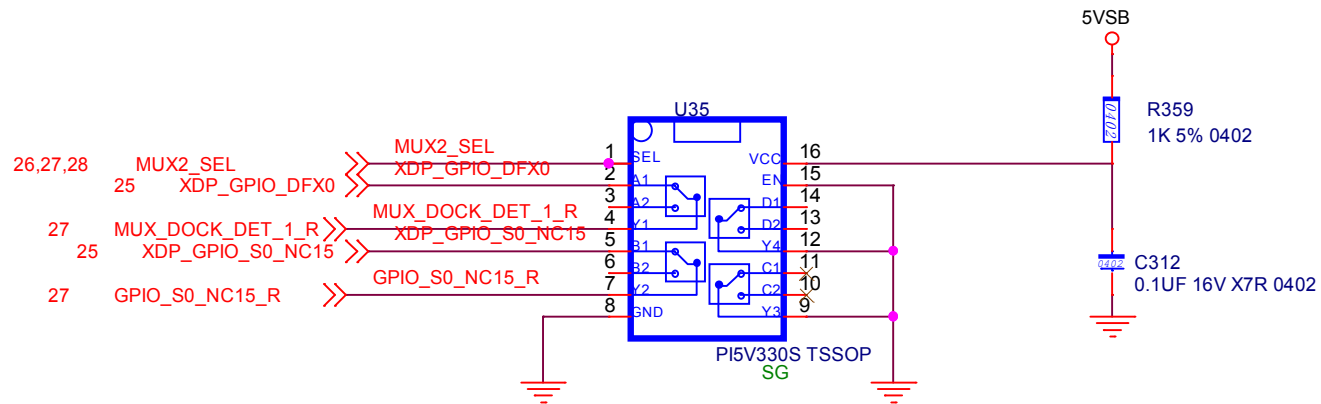


R339 placed close to XDP CONN
R335, R336, R337, R338, placed close to the Soc

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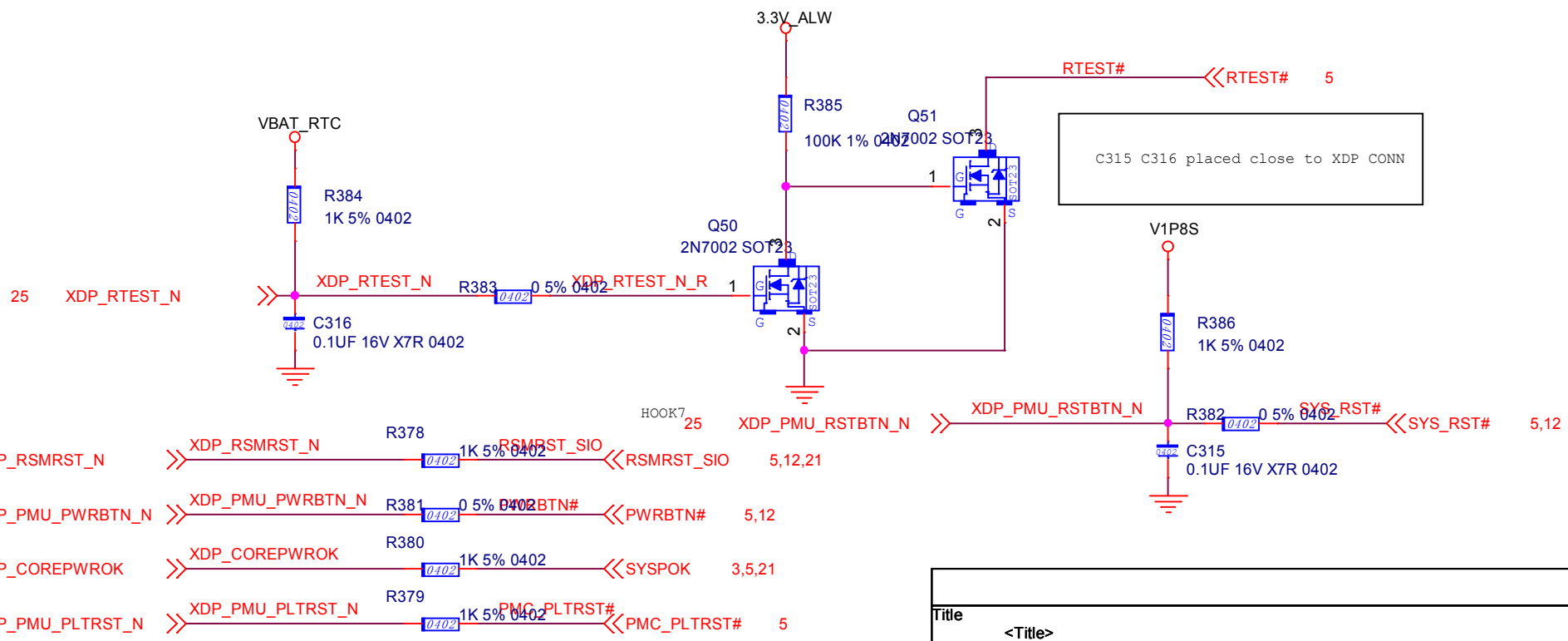
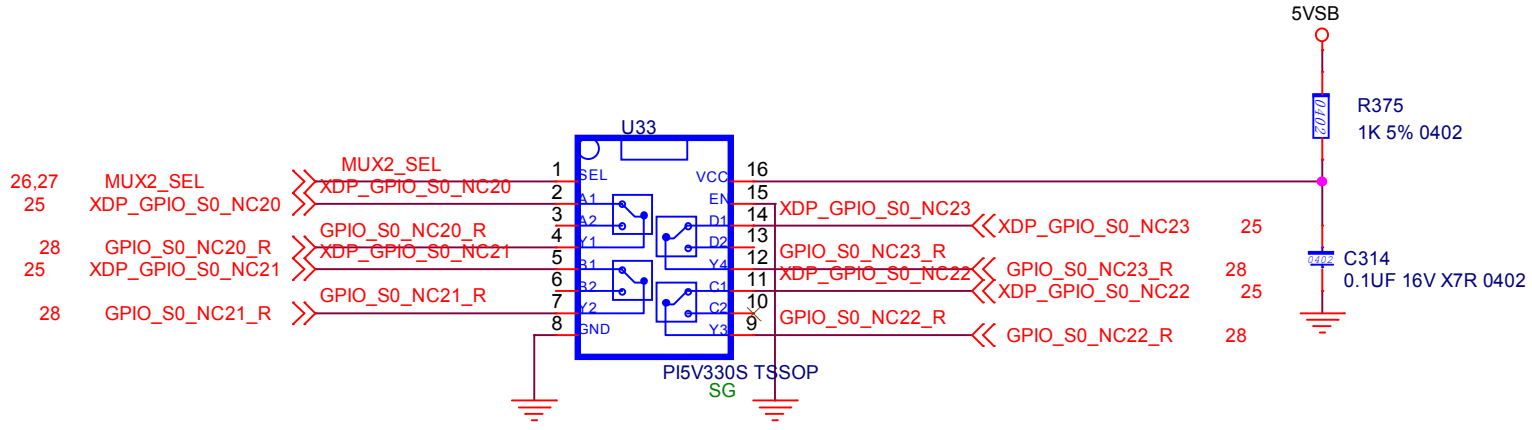


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4	GPIO_S0_NC20	GPIO_S0_NC20	R372	0 5% 0402	GPIO_S0_NC20_R	28
4	GPIO_S0_NC21	GPIO_S0_NC21	R371	0 5% 0402	GPIO_S0_NC21_R	28
4	GPIO_S0_NC22	GPIO_S0_NC22	R373	0 5% 0402	GPIO_S0_NC22_R	28
4	GPIO_S0_NC23	GPIO_S0_NC23	R374	0 5% 0402	GPIO_S0_NC23_R	28



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